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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: TIJ-18438
Takahiro Miyazaki
Serial No: 08/324,835
Filed: October 18, 1994
For: OVERDRIVE CIRCUIT

Art Unit: 2107
Examiner: A. Paladini

ASSISTANT COMMISSIONER FOR PATENTS
Washington, DC 20231

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William E. Hiller
William E. Hiller
Attorney for Applicant
Registration No. 18,803

Texas Instruments Incorporated
P.O. Box 655474, M/S 219
Dallas, TX 7526
October 8, 1996

CERTIFICATE OF MAILING
37 CFR 1.8(a)

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: ASSISANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231 ON THE DATE BELOW.

Oct. 8, 1996
DATE

William E. Hiller
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APPEAL BRIEF

Assistant Commissioner for Patents
Washington, DC 20231

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I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on October 8, 1996.

William E. Hiller

William E. Hiller, Reg. No. 18,803

Sir:

This is an appeal from the final rejection of Claims 2-10 as set forth in the Office Action dated February 6, 1996.

Real Party in Interest

Texas Instruments Incorporated of Dallas, Texas is the real party in interest with respect to this application on appeal by virtue of an assignment to Texas Instruments Incorporated from Texas Instruments Japan, Ltd. and the sole applicant, Takahiro Miyazaki, of the entire right, title and interest in and to the claimed invention in this application on appeal. The assignment to Texas Instruments Incorporated from Texas Instruments Japan, Ltd. and the sole applicant, Takahiro Miyazaki, was recorded in the U.S. Patent and Trademark Office on Reel 7256, Frames 293-295 on December 19, 1994.

Related Appeals and Interferences

None.

Status of the Claims

Claim 1 has been cancelled.

Claims 2-10, inclusive, have been finally rejected, and are the claims presented in this appeal.

Status of Amendment Filed Subsequent to Final Rejection

No amendment has been filed subsequent to the Office Action dated February 6, 1996 in which Claims 2-10, inclusive, were finally rejected.

Summary of Invention

The invention as defined by the claims on appeal is directed to an integrated overdrive circuit formed on a single semiconductor chip, wherein the overdrive circuit is capable of operating switching elements external to the semiconductor chip, such as a switching element in a switching regulator, at a high rate of speed.

The overdrive circuit includes first and second current sources PG_{12} and PG_{11} for respectively supplying first and second currents I_{PG12} and I_{PG11}, wherein the second current I_{PG11} supplied by the second current source is smaller in magnitude than the first current I_{PG12} as supplied by the first current source. The first current source provides the first current as an overdrive current for driving a switching element, and is regulated by a first circuit connected thereto and operating the first current source for a predetermined time period in providing the first current. The overdrive circuit further includes a second circuit which is connected to the first circuit and stops the operation of the first circuit after the predetermined time period within which the first current is to be provided has elapsed so as to stop the first current source from providing the overdrive current. The second circuit is also connected to the second current source and operates the second current source to provide the second current as an ordinary current for driving the switching element.

(Specification - page 4, last paragraph - page 5, line 19; Figs. 1, 3 and 4)

Typically, the use of a bipolar transistor as a switching element external to an integrated overdrive circuit, will require a change in collector voltage (either higher or lower) at high speed. To accomplish such high speed operation of the external bipolar transistor, the base current thereof has been temporarily increased by adding an external capacitor to the integrated overdrive circuit. While the addition of the external capacitor enables high speed operation of the external switching element by the integrated overdrive circuit to be accomplished, the trend in electronic portable equipment, such as video cameras, is to eliminate as many external parts of the integrated overdrive circuit as possible without a consequent increase in the chip area of the integrated circuit or the cost thereof which would inevitably result by providing a capacitor capable of producing several tens to several hundred pF as the needed capacitance and within the integrated overdrive circuit. (Specification - page 1 (line 4 is blank), lines 6-12; page 4, lines 4-22)

The integrated overdrive circuit comprising the claimed subject matter on appeal provides an induced overdrive current without requiring an external capacitor such that the number of external components are thereby reduced while also avoiding an increase in the chip area or the cost of the integrated overdrive circuit.

To this end, in a specific aspect of the invention as defined by the claims on appeal, the first current source PG_{12} is formed by a first plurality of bipolar transistors P_{121}, P_{122}, and P_{123} having respective base, collector and emitter electrodes and arranged in parallel relationship with respect to each other with the bases, collectors and emitters of the first plurality of bipolar transistors being respectively connected together. The first circuit connected to the first current source PG_{12} includes a bipolar transistor Q_{12} having base, collector and emitter electrodes. The base of the bipolar transistor Q_{12} included in the

first circuit is connected to the voltage supply source V_{cc}, and its collector is connected to the commonly connected bases of the bipolar transistors P_{121}, P_{122} and P_{123} of the first current source PG_{12}. The first circuit bipolar transistor Q_{12} is conductive over a predetermined time period for rendering the first plurality of bipolar transistors P_{121}, P_{122} and P_{123} of the first current source PG_{12} conductive, thereby providing a first current I_{PG12} as the overdrive current for driving the externally located switching element QPT_1 by raising the voltage of the base electrode of the bipolar transistor defining the switching element QPT_1.

A second current source PG_{11} which supplies a second current I_{PG11} smaller in magnitude than the first current I_{PG12} includes a second plurality of bipolar transistors P_{111}. P_{112} and P_{113} having base, collector and emitter electrodes and arranged in parallel relationship with respect to each other with the bases, collectors and emitters of the second plurality of bipolar transistors P_{111}, P_{112} and P_{113} being respectively connected together.

The second circuit includes a second circuit bipolar transistor Q_{11} having base, collector and emitter electrodes, with the base of the second circuit bipolar transistor Q_{11} being connectable to the voltage supply source V_{cc} and the collector of the second circuit bipolar transistor Q_{11} being connected to a node located in the connection between the voltage supply source V_{cc} and the base of the first circuit bipolar transistor Q_{12}.

Initially, upon the energization of a current source I_{e11}, the electric potential of a node ND_1 connected between the current source I_{e11} and the voltage supply source V_{cc} falls, thereby causing the bipolar transistor Q_{12} of the first circuit to become conductive. In this respect, the bipolar transistor Q_{12} of the first circuit becomes conductive prior to the second bipolar transistor Q_{11} of the second circuit as the voltage at the node ND_1 begins to decrease, with current flowing in the emitter of the bipolar transistor Q_{12} of the first circuit until the potential of the node ND_1 equals $(V_{cc} - 2\ V_{se})$. During the period of time that the bipolar transistor Q_{12} of the first circuit is conductive, the

collector of the bipolar transistor Q_{12} delivers current to the commonly connected bases of the transistors P_{121}, P_{122}, and P_{123} of the first current source PG_{12}, thereby turning on the transistors P_{121}, P_{122}, and P_{123} and allowing a first current I_{PG12} to flow to a current mirror circuit MR and hence to the base of the transistor QPT_1 defining the switching element as overdrive current such that the high speed operation of the bipolar transistor QPT_1 defining the switching element will be achieved.

As the electric potential at the node ND_1 falls further to reach the level $(V_{cc} - 2\ V_{BE})$, the bipolar transistor Q_{11} of the second circuit will be turned on, such that current will be drawn from a node between the power supply voltage V_{cc} and the base of the bipolar transistor Q_{12} of the first circuit by the collector of the bipolar transistor Q_{11} of the second circuit, causing the potential at the base of the transistor Q_{12} to fall and turning off the transistor Q_{12}. Consequently, each of the bipolar transistors P_{121}, P_{122}, and P_{123} is turned off to shut down the first current source PG_{12}. Therefore, the overdrive current I_{PG12} is shut off.

However, the bipolar transistor Q_{11} of the second circuit having a collector connected to the commonly connected bases of the bipolar transistors P_{111}, P_{112}, and P_{113} of the second current source PG_{11} turns on the transistors P_{111}, P_{112}, and P_{113} such that a second current I_{PG11} is provided from the second current source of a magnitude less than the first current I_{PG12}, the second current I_{PG11} providing ordinary current to the base of the bipolar transistor QPT_1 defining the external switching element. (Specification - page 8, line 15 - page 9 (line 4 is blank), line 35)

The overdrive circuit may further include first and second resistors R_{14} and R_{12} respectively disposed in the connection between the voltage supply source V_{cc} and the first and second current sources PG_{12} and PG_{11}, with the first resistor R_{14} determining the magnitude of the overdrive current I_{PG12} provided by the first current source PG_{12}, and the second resistor R_{12} determining the magnitude of the ordinary current I_{PG11} provided by

the second current source PG_{11}. (Specification - page 10 (lines 7 and 8 are blank), lines 19-21)

In a further specific aspect of the overdrive circuit, the outputs of the first and second current sources PG_{12} and PG_{11} are connected to a common node to which the input of a current mirror circuit MR is connected. The output of the current mirror circuit MR is connected to an output terminal T_1 which is adapted to be connected to the switching element to be driven, such as the base of the bipolar transistor QPT_1. The current mirror circuit includes a plurality of bipolar transistors Q_{M13}, Q_{M14}, and Q_{M15} having base, collector and emitter electrodes which are commonly connected. The current mirror circuit MR further includes an actuator bipolar transistor Q_{Mi1} having base, collector and emitter electrodes, with the collector of the actuator bipolar transistor Q_{Mi1} being connectable to the voltage supply source V_{cc}, and the base of the actuator bipolar transistor Q_{Mi1} being connected to the common node to which the outputs of the first and second current sources PG_{12} and PG_{11} are connected. The emitter of the actuator bipolar transistor Q_{mi1} is connected to the commonly connected bases of the plurality of bipolar transistors Q_{M13}, Q_{M14}, and Q_{M15} included in the current mirror circuit MR. If either the first current I_{PG12} or the second current I_{PG11} is applied to the base of the actuator bipolar transistor Q_{Mi1}, the actuator bipolar transistor Q_{Mi1} becomes conductive and turns on the bipolar transistors Q_{M12}, Q_{M14}, and Q_{M15}, thereby rendering the current mirror circuit MR operative to provide a driving current at the output terminal T_1. (Specification - page 7, line 1 - page 8, line 14; page 9 (line 4 is blank), lines 15-21)

In another embodiment of the overdrive circuit, the current mirror circuit may comprise a single bipolar transistor Q_{M16} (Figure 3) whose base is connected to the common node to which the outputs of the first and second current sources PG_{12} and PG_{11} are connected. The application of either of the first or second currents PG_{12} or PG_{11} to the base of the bipolar transistor Q_{M16} renders the bipolar transistor Q_{M16} conductive, thereby providing a

driving current at the output terminal T_1. (Specification - page 11, line 26 - page 12, line 7)

In the embodiment of the overdrive circuit illustrated in Figure 1, npn transistors Q_{M13}, Q_{M14}, and Q_{M15} are included in the current mirror circuit MR and provide an output via the commonly connected collectors thereof to the output terminal T_1. Conversely, in the embodiment of Figure 4, the bipolar transistors Q_{M13}, Q_{M14}, and Q_{M15} of the current mirror circuit MR provide an output via the commonly connected emitters thereof to the output terminal T_1.

The overdrive circuit as defined by the claims on appeal thereby has the capability of providing an overdrive current for driving an externally located switching transistor (in a switching regulator, for example) for high speed operation of the switching transistor without requiring a capacitor external to the integrated circuit chip on which the overdrive circuit is present. Furthermore, this is accomplished without an increase in the chip area or the cost of the integrated overdrive circuit thereon.

References Relied Upon by Examiner

U.S. Patent	Patentee	Issue Date
4,925,156	Stoll et al	May 15, 1990
5,053,911	Kopec et al	October 1, 1991

Issue Presented for Review

Whether Claims 2-10 (sic "Claim 1") are properly rejected under 35 USC 103 as being unpatentable over Stoll et al in view of Kopec et al.

Appellant states for the record that Claims 2-10 on appeal do not stand or fall together when considering the final rejection thereof. Arguments supporting the independent patentability of Claims 2-10, inclusive, are set forth in the following section.

Arguments Supporting Appeal

The Office Action of February 6, 1996 constituting a final rejection of this application on appeal, refers on page 3 thereof to a rejection of "Claim 1 ..." under 35 USC 103 as being unpatentable over Stoll et al in view of Kopec et al. Claim 1 is no longer in this application, being cancelled in amendment A filed December 18, 1995. It is apparent from the summary page of the Office Action of February 6, 1996 that Claims 2-10, inclusive, were intended by the Examiner to be the "rejected" claims under 35 USC 103 as allegedly being unpatentable over Stoll et al in view of Kopec et al. Independent Claim 2 from each of Claims 3-10, inclusive, is dependent in varying sequences, defines an integrated overdrive circuit formed on a single semiconductor chip which requires "a first current source" and "a second current source" in combination with "a first circuit" and "a second circuit" which are interrelated in such a manner as to clearly patentably distinguish over Stoll et al, whether considered singly or in combination with Kopec et al. Referring to Stoll et al, it will be observed that the control circuit disclosed therein requires a capacitor 20 as a component thereof. The capacitor 20 is charged so as to provide a voltage to an astable multivibrator defined by NAND gate 21, resistors 22, 23, diode 24 and capacitor 25. It is respectfully submitted that Stoll et al does not suggest or teach "a first current source" and "a second current source" interrelated with "a first circuit" and "a second circuit" in the manner required by Claim 2.

The Examiner appears to concede the shortcomings of Stoll et al in the latter respect, but relies upon Kopec et al as purportedly suggesting in Figure 1 two current sources I_1 and I_2 for operating a switching element S1. It is the Examiner's position that it would be obvious to add the two current source systems of Kopec et al to the switch control system of Stoll et al as a basis for finally rejecting Claims 2-10, inclusive. It is respectfully urged that the proposed combination of Stoll et al in view of Kopec et al advanced by the Examiner as a basis of final

rejection is inappropriate for teaching or suggesting the integrated overdrive circuit defined in Claim 2 on appeal. In Kopec et al, the two current sources I_1 and I_2 are reference current sources alternatively actuated by closure of the respective switch SA or SB associated therewith to provide either current I_1 or I_2 to one input of a comparator 22. The other input of the comparator 22 is taken from an amplifier 18 which senses the current through a coil 12 of a solenoid 10. Accordingly, it is insisted that the purpose of Kopec et al in utilizing a comparator 22 for controlling the opening and closing of a switch S1 represents a structural and functional arrangement clearly different from what is defined in Claim 2 on appeal. Moreover, there is no suggestion in either of Stoll et al or Kopec et al for modifying Stoll et al in the manner proposed by the Examiner, any such suggestion coming from appellant's own disclosure and amounting to improper "hindsight". Furthermore, it could not be said that Kopec et al employs "a first circuit" and "a second circuit" in conjunction with the first and second reference current sources shown therein operating in the manner required by Claim 2. The overdrive circuit of Claim 2 is an integrated circuit provided on a single semiconductor chip which is capable of achieving an overdrive current to enable operation of a switching element (i.e. bipolar transistor) located off-chip without requiring a capacitor either on the chip or external thereto to temporarily increase the base current of the external transistor. This is precisely contrary to the showing in Stoll et al where the capacitor 20 is employed for charging an input to the NAND gate 21 to enable the output of the NAND gate 21 to change from "1" to "0", thereby turning off the transistor 27 by removing the current applied to the base electrode thereof. Therefore, regardless of the modification of Stoll et al as proposed by the Examiner to purportedly add first and second current sources on the basis of the showing in Kopec et al, the resultant hypothetical structure would still require the presence of the capacitor 20 in order to be operative, in contrast to the

overdrive circuit comprising the claimed subject matter on appeal in this application.

In addition, Claim 2 requires the "first circuit" to be "connected to said first current source and operating said first current source for a predetermined time period to provide the first current as an overdrive current ..." in conjunction with a "second circuit connected to said first circuit for stopping the operation of said first circuit after the predetermined time period has elapsed to stop said first current source from providing the overdrive current", with the "second circuit" also being "connected to said second current source and operating said second current source to provide the second current as an ordinary current ...". In no sense could it be said that the two current sources providing the reference currents I_1 and I_2 as disclosed in Kopec et al are operable in the manner required in Claim 2. In the latter respect, Kopec et al does not provide a "first circuit" and a "second circuit" interrelated with the current sources SA and SB and controlling the provision of a first current and a second current therefrom in the manner specifically required in Claim 2. It follows that, however considered, the combination of Stoll et al and Kopec et al could not produce a hypothetical structure similar to that defined in Claim 2.

Claims 3-10, inclusive, being dependent from Claim 2 in varying sequences, are thereby urged to distinguish over the collective teachings of Stoll et al and Kopec et al in a non-obvious patentable manner similar to that argued on behalf of Claim 2. Claim 3, dependent from Claim 2, further structurally restricts the "first current source" as comprising "a first plurality of bipolar transistors having respective base, collector and emitter electrodes and arranged in parallel relationship with respect to each other with the bases, collectors and emitters of the first plurality of bipolar transistors being respectively connected together". The "first circuit" is further structurally restricted in Claim 3 to require "a bipolar transistor having base, collector and emitter electrodes, the base of said first

circuit bipolar transistor being connectable to a voltage supply source and having the collector thereof connected to the commonly connected bases of said first plurality of bipolar transistors of said first current source". Thus, while the "first circuit bipolar transistor" is "conductive over the predetermined time period", the first plurality of bipolar transistors are rendered conductive "so as to provide the first current as the overdrive current for driving the switching element". It is respectfully submitted that nothing even remotely comparable to such structure can be found in either of Stoll et al or Kopec et al. For this further reason, it is considered that Claim 3 patentably distinguishes over the collective teachings of Stoll et al and Kopec et al.

Claim 4 depends from Claims 3 and 2 in sequence and further structurally restricts the "second current source" as comprising "a second plurality of bipolar transistors having base, collector and emitter electrodes and arranged in parallel relationship with respect to each other with the bases, collectors and emitters of the second plurality of bipolar transistors being respectively connected together", while the "second circuit" is further structurally defined as including "a second circuit bipolar transistor having base, collector and emitter electrodes, the base of said second current bipolar transistor being connectable to the voltage supply source, and the collector of said second current bipolar transistor being connected to a node located in the connection between the voltage supply source and the base of said first circuit bipolar transistor". Thus, the "second circuit bipolar transistor" becomes conductive "in response to a rise in voltage at the base thereof" so as to draw "current from the voltage supply source through the collector thereof so as to lower the voltage supplied to the base of said first circuit bipolar transistor for turning off said first circuit bipolar transistor to render said first circuit bipolar transistor nonconductive". This causes "the first plurality of bipolar transistors defining said first current source" to become "nonconductive to stop said

first current source from providing the overdrive current in response to said first circuit bipolar transistor being rendered nonconductive". As this occurs, the "second circuit bipolar transistor" becomes conductive so as to render "said second plurality of bipolar transistors defining said second current source conductive so as to operate said second current source to provide the second current as the ordinary current for driving the switching element". None of the structural features added by Claim 4 can be found in either of Stoll et al or Kopec et al. For this further reason, Claim 4 is considered to patentably distinguish over the collective teachings of Stoll et al and Kopec et al.

Claim 5 depends from Claim 2, and further requires "first and second resistors respectively disposed in the connection between the voltage supply source and said first and second current sources". In this connection, the "first resistor" is "determinative of the magnitude of the overdrive current provided by said first current source" and the "second resistor" is "determinative of the magnitude of the ordinary current provided by said second current source". This structural feature is another departure from what can be found in Kopec et al which shows simply on-off switches SA and SB as a means of providing a reference current level which may be either I_1 or I_2 depending upon which of the switches SA and SB is closed during a given instant of time.

Claim 6 also depends from Claim 2 and requires "a current mirror circuit ... the input of said current mirror circuit being connected to the common node to which the outputs of said first and second current sources are connected" in conjunction with "an output terminal connected to the output of said current mirror circuit ...". There is no current mirror circuit disclosed or suggested in either of Stoll et al or Kopec et al. For this reason, it is respectfully urged that Claim 6 further patentably distinguishes over the collective teachings of Stoll et al and Kopec et al.

Claim 7 depends from Claims 6 and 2 in sequence, and further structurally restricts the "current mirror circuit" as defined in Claim 6 to include "a plurality of bipolar transistors having commonly connected base, collector and emitter electrodes" and "an actuator bipolar transistor having base, collector and emitter electrodes", wherein "the collector of said actuator bipolar transistor" is "connectable to the voltage supply source, the base of said actuator bipolar transistor being connected to the common node connecting the outputs of said first and second current sources, and the emitter being connected to the commonly connected bases of said plurality of bipolar transistors included in said current mirror circuit". Thus, the "actuator bipolar transistor" is "rendered conductive in response to the application of either of the first or second current ... to the base thereof to turn on said plurality of bipolar transistors for rendering said current mirror circuit operative to provide a driving current at the output terminal". Nothing comparable to such structure is taught or suggested by either of Stoll et al or Kopec et al.

Claim 8 depends from Claims 6 and 2 in sequence, and is readable upon the embodiment of the invention illustrated in Figure 3 in defining the "current mirror circuit" as comprising "a single bipolar transistor having base, collector and emitter electrodes" with "the base of said single bipolar transistor defining said current mirror circuit being connected to the common node to which the outputs of said first and second current sources are connected" such that the "single bipolar transistor defining said current mirror source" is "rendered conductive in response to the application of either of the first or second currents as respectively provided by said first and second current sources to the base thereof to provide a driving current at the output terminal". Such structure is yet another departure from anything to be found in either of Stoll et al or Kopec et al, and enhances the patentability of Claim 8, in addition to the patentably distinguishing structural features recited in parent Claims 6 and 2 from which Claim 8 depends in sequence.

Claims 9 and 10 respectively depend from Claims 7, 6 and 2 in sequence and are directed to different structural versions of the "current mirror circuit" as to the output therefrom which is applied to the output terminal "via the collectors" (Claim 9) or "via the emitters" (Claim 10) "of said plurality of bipolar transistors included in said current mirror circuit", thereby being readable upon the embodiments shown in Figures 1 and 4 of the drawings respectively. The structural features added by Claims 9 and 10 are yet further distinguishing features over the collective teachings of Stoll et al and Kopec et al, thereby enhancing the patentability of Claims 9 and 10.

Summation

Claims 2-10, inclusive, on appeal are urged to distinguish in a non-obvious patentable manner over the collective teachings of Stoll et al and Kopec et al, as combined by the Examiner for purposes of final rejection under 35 USC 103. It is believed that essentially all of the structural interrelationships defined in Claims 2-10, inclusive, are not obvious from the disclosure of Stoll et al as purportedly modified by Kopec et al in the manner proposed by the Examiner. Accordingly, the Honorable Board of Patent Appeals and Interferences is respectfully requested to reverse the final rejection of Claims 2-10, inclusive, on appeal on the basis of the arguments as presented herein.

Respectfully submitted,

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October 8, 1996
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APPENDIX - CLAIMS ON APPEAL

--2. An integrated overdrive circuit formed on a single semiconductor chip comprising:

a first current source for supplying a first current;

a first circuit connected to said first current source and operating said first current source for a predetermined time period to provide the first current as an overdrive current for driving a switching element;

a second current source for supplying a second current smaller in magnitude than the first current; and

a second circuit connected to said first circuit for stopping the operation of said first circuit after the predetermined time period has elapsed to stop said first current source from providing the overdrive current;

said second circuit also being connected to said second current source and operating said second current source to provide the second current as an ordinary current for driving the switching element.--

--3. An overdrive circuit as set forth in Claim 2, wherein said first current source comprises a first plurality of bipolar transistors having respective base, collector and emitter electrodes and arranged in parallel relationship with respect to each other with the bases, collectors and emitters of the first

plurality of bipolar transistors being respectively connected together;

said first circuit connected to said first current source including a bipolar transistor having base, collector and emitter electrodes, the base of said first circuit bipolar transistor being connectable to a voltage supply source and having the collector thereof connected to the commonly connected bases of said first plurality of bipolar transistors of said first current source; and

said first circuit bipolar transistor being conductive over the predetermined time period for rendering the first plurality of bipolar transistors included in said first current source conductive so as to provide the first current as the overdrive current for driving the switching element.--

--4. An overdrive circuit as set forth in Claim 3, wherein said second current source for supplying the second current smaller in magnitude than the first current comprises a second plurality of bipolar transistors having base, collector and emitter electrodes and arranged in parallel relationship with respect to each other with the bases, collectors and emitters of the second plurality of bipolar transistors being respectively connected together;

said second circuit including a second circuit bipolar transistor having base, collector and emitter electrodes, the base of said second circuit bipolar transistor being connectable to the voltage supply source, and the collector of said second circuit bipolar transistor being connected to a node located in the connection between the voltage supply source and the base of said first circuit bipolar transistor;

said second circuit bipolar transistor being rendered conductive in response to a rise in voltage at the base thereof and drawing current from the voltage supply source through the

collector thereof so as to lower the voltage applied to the base of said first circuit bipolar transistor for turning off said first circuit bipolar transistor to render said first circuit bipolar transistor nonconductive;

said first plurality of bipolar transistors defining said first current source being rendered nonconductive to stop said first current source from providing the overdrive current in response to said first circuit bipolar transistor being rendered nonconductive; and

said second circuit bipolar transistor, when conductive, rendering said second plurality of bipolar transistors defining said second current source conductive so as to operate said second current source to provide the second current as the ordinary current for driving the switching element.--

--5. An overdrive circuit as set forth in Claim 2, further including first and second resistors respectively disposed in the connection between the voltage supply source and said first and second current sources;

said first resistor being determinative of the magnitude of the overdrive current provided by said first current source, and said second resistor being determinative of the magnitude of the ordinary current provided by said second current source.--

--6. An overdrive circuit as set forth in Claim 2, wherein said first and second current sources have their respective outputs connected to a common node;

a current mirror circuit having an input and an output, the input of said current mirror circuit being connected to the common node to which the outputs of said first and second current sources are connected; and

an output terminal connected to the output of said current mirror source and adapted to be connected to the switching element to be driven.--

--7. An overdrive circuit as set forth in Claim 6, wherein said current mirror circuit includes a plurality of bipolar transistors having commonly connected base, collector and emitter electrodes; and

an actuator bipolar transistor having base, collector and emitter electrodes, the collector of said actuator bipolar transistor being connectable to the voltage supply source, the base of said actuator bipolar transistor being connected to the common node connecting the outputs of said first and second current sources, and the emitter being connected to the commonly connected bases of said plurality of bipolar transistors included in said current mirror circuit;

said actuator bipolar transistor being rendered conductive in response to the application of either of the first or second current as respectively provided by said first and second current sources to the base thereof to turn on said plurality of bipolar transistors for rendering said current mirror circuit operative to provide a driving current at the output terminal.--

--8. An overdrive circuit as set forth in Claim 6, wherein said current mirror circuit comprises a single bipolar transistor having base, collector and emitter electrodes;

the base of said single bipolar transistor defining said current mirror circuit being connected to the common node to which the outputs of said first and second current sources are connected; and

said single bipolar transistor defining said current mirror circuit being rendered conductive in response to the application of either of the first or second current as respectively provided

by said first and second current sources to the base thereof to provide a driving current at the output terminal.--

--9. An overdrive circuit as set forth in Claim 7, wherein the output from said current mirror circuit is applied to said output terminal via the collectors of said plurality of bipolar transistors included in said current mirror circuit.--

--10. An overdrive circuit as set forth in Claim 7, wherein the output from said current mirror circuit is applied to said output terminal via the emitters of said plurality of bipolar transistors included in said current mirror circuit.--

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